

Application No.: 09/938,672

Docket No.: M4065.0475/P475

AMENDMENT TO THE CLAIMS

1-16 (Cancelled)

17. (Currently Amended) A method of fabricating a memory device comprising:

forming a first memory cell to include comprising a resistance-changeable chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material between and electrically coupled to a first electrode and a second electrode; and

forming a second memory cells as a ~~common~~ mode to include cell comprising a resistance-changeable chalcogenide glass material having a changeable resistance and ~~cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material~~ between and electrically coupled to said second electrode and a third electrode;

~~forming said anode electrodes of said memory cells as a common anode, wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer~~ second electrode comprises a first silver layer, a tungsten layer over said first silver layer, and a second silver layer over said tungsten layer.

18. (Currently Amended) A method as in claim 17 further comprising: ~~forming vertically stacking said first memory cell such that it is stacked on and~~ said second memory cell.

19. (Currently Amended) A method as in claim 17 further comprising: ~~forming each of said first and second memory cells of a layered structure which includes a cathode layer, a chalcogenide glass material layer having a changeable resistance and a anode layer, wherein said first and third electrodes each comprise a layer of tungsten and a layer of tungsten nitride.~~

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20. (Currently Amended) A method as in claim 17, wherein each of said ~~cathodes~~ first and third electrodes comprises ~~a~~ at least one layer of tungsten, platinum, titanium, cobalt, aluminum, or nickel.

21. (Cancelled)

22. (Currently Amended) A method as in claim 17, wherein said ~~middle conductive layer comprises tungsten~~ first electrode, said second electrode, and said third electrode are each electrically coupled to a voltage source or to a read circuit.

23. (Currently Amended) A method as in claim 18 further comprising: forming said stacked first and second memory cells over a conductive plug such that said ~~cathode~~ first electrode of said ~~second~~ first memory cell is ~~in~~ electrically coupled ~~with~~ to said conductive plug.

24. (Currently Amended) A method as in claim ~~23~~ 18 further comprising:
forming a first row line conductor ~~electrically coupled to a second active region of a first access transistor~~ to control current flow between a first column line and said first electrode;

forming a second row line conductor to control current flow between a second column line and said third electrode; and

forming a sense amplifier circuit electrically coupled to said second electrode.

25. (Currently Amended) A method as in claim ~~23~~ 17, further comprising ~~forming a word line conductor which is electrically coupled to a gate of a first access transistor~~ wherein said chalcogenide glass material of said first and second memory cells comprises germanium selenide.

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26. (Currently Amended) A method as in claim ~~23~~ 25, further comprising forming a second access transistor and electrically coupling said second access transistor to said second memory cell wherein said germanium selenide has the formula $(\text{Ge}_x\text{Se}_{1-x}) + \text{Ag}$.

27. (Currently Amended) A method as in claim ~~26~~ 17, wherein said first and second memory cells are formed to be coupled to different column lines by said respective first and second access transistors.

28. (Currently Amended) A method as in claim 17, wherein said first and second memory cells are formed to be connected to the same electrically coupled to a single column line by said respective first and second access transistors.

29. (Currently Amended) A method as in claim ~~26~~ 28 further comprising: forming a circuit for operating said first and second access transistors separately to individually access each of said first and second memory cells.

30. (Currently Amended) A method as in claim ~~17~~ 28 further comprising: forming a circuit for operating said first and second access transistors together to access both said first and second memory cells simultaneously.

31-57. (Cancelled)

58. (Currently Added) A method of forming a memory device comprising:

forming a first electrode, said first electrode comprising a material selected from the group consisting of tungsten, tungsten nitride, platinum, titanium, cobalt, aluminum, and nickel;

forming a first germanium selenide layer over and electrically coupled said first electrode;

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incorporating a first silver-containing material into said first germanium selenide layer;

forming a first silver layer over and electrically coupled to said first germanium selenide layer;

forming a tungsten layer over and electrically coupled to said first silver layer;

forming a second silver layer over and electrically coupled to said tungsten layer;

forming a second germanium selenide layer over and electrically coupled to said second silver layer;

incorporating a second silver-containing material into said second germanium selenide layer; and

forming a second electrode over and electrically coupled to said second germanium selenide layer, said second electrode comprising a material selected from the group consisting of tungsten, tungsten nitride, platinum, titanium, cobalt, aluminum, and nickel.

59. (Currently Added) A method of fabricating a memory device comprising:

forming a first memory cell comprising a resistance-changeable chalcogenide glass material between and electrically coupled to a first electrode and a second electrode;

forming a second memory cell comprising a resistance-changeable chalcogenide glass material between and electrically coupled to said second electrode and a third electrode;

providing a first access circuit for said first memory cell, said first access circuit comprising a first column line, a first row line, and a first access transistor having a gate

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coupled to said first row line and configured to electrically couple said first electrode to said first column line; and

providing a second address circuit for said second memory cell, said second address circuit comprising a second column line, a second row line, and a second access transistor having a gate coupled to said second row line and configured to electrically couple said third electrode to said second column line.

60. (Currently Added) The method of claim 59, further comprising providing a first sense amplifier circuit electrically coupled to said first column line and a second sense amplifier circuit electrically coupled to said second column line.

61. (Currently Added) The method of claim 60, further comprising:

providing a third transistor between said first column line and said first sense amplifier circuit; and

providing a fourth transistor between said second column line and said second sense amplifier circuit.

62. (Currently Added) The method of claim 59, further comprising providing a sense amplifier circuit electrically coupled to said second electrode.